

Fig. 1.
(Prior Art)

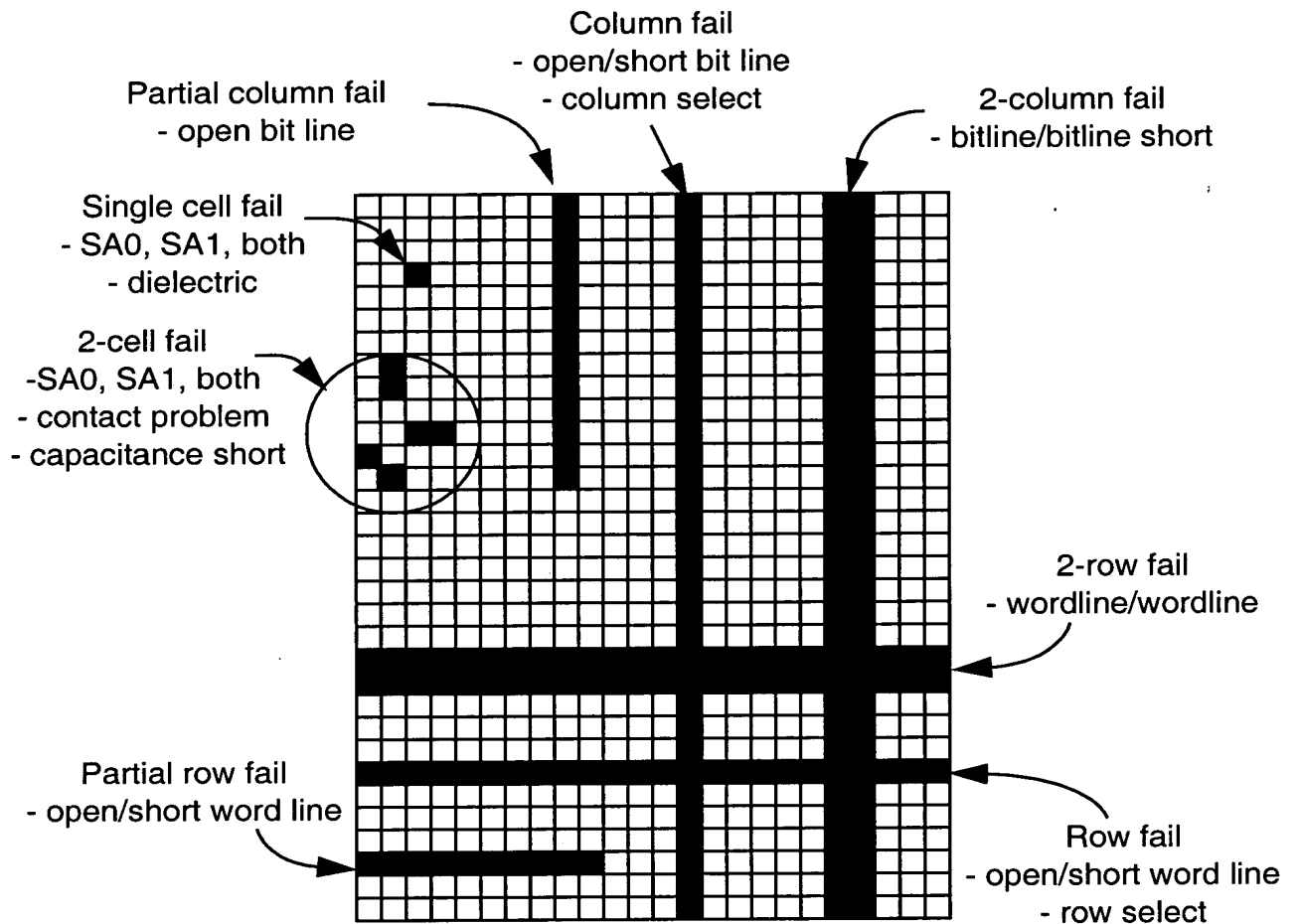
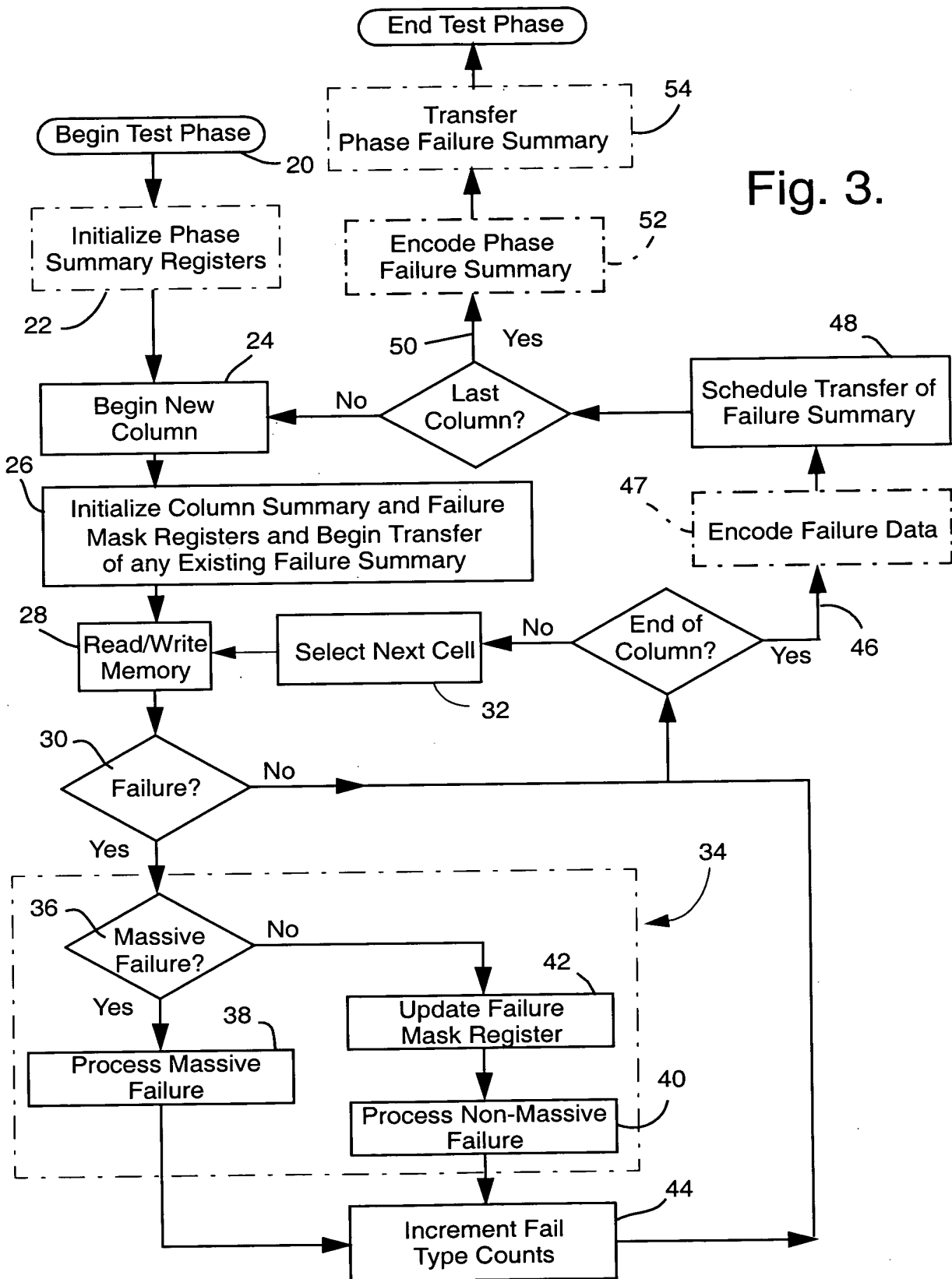
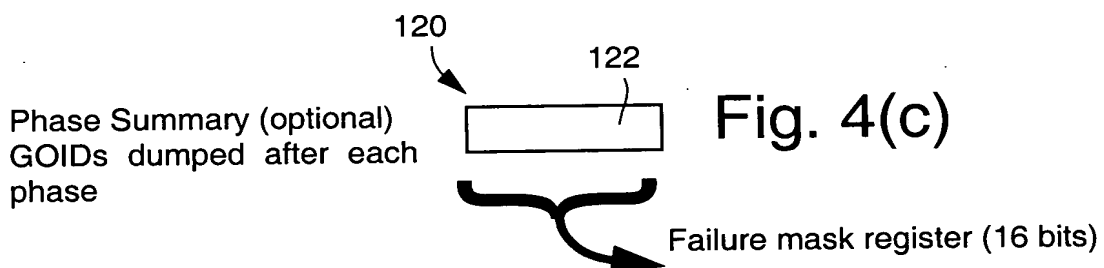
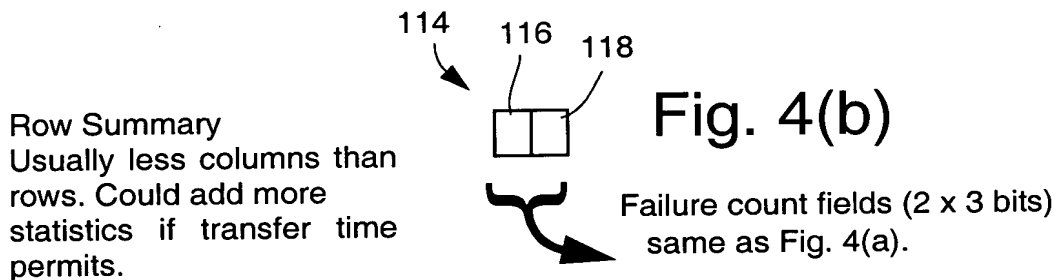
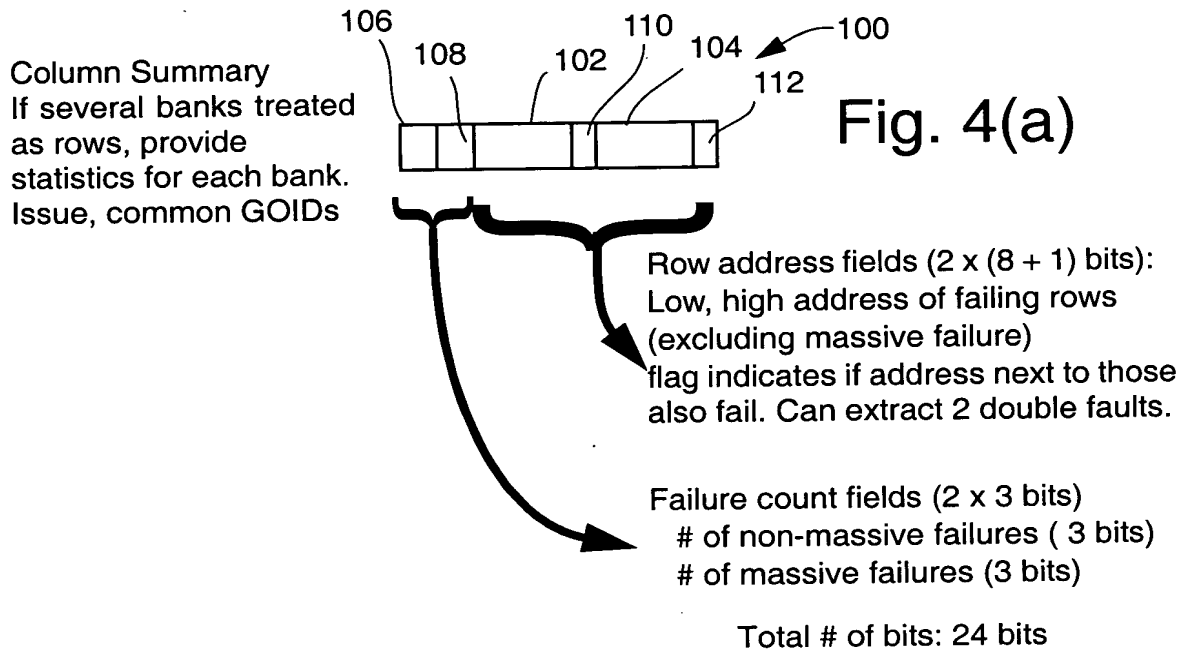


Fig. 2
(Prior Art)



Column summary contains row addresses of first and last failure and failure counts
 Row summary contains at least failure counts
 Phase summary contains failure mask register information
 Test is rerun for each failing bit of failure mask register



Column summary contains (for each of 2 address segments):

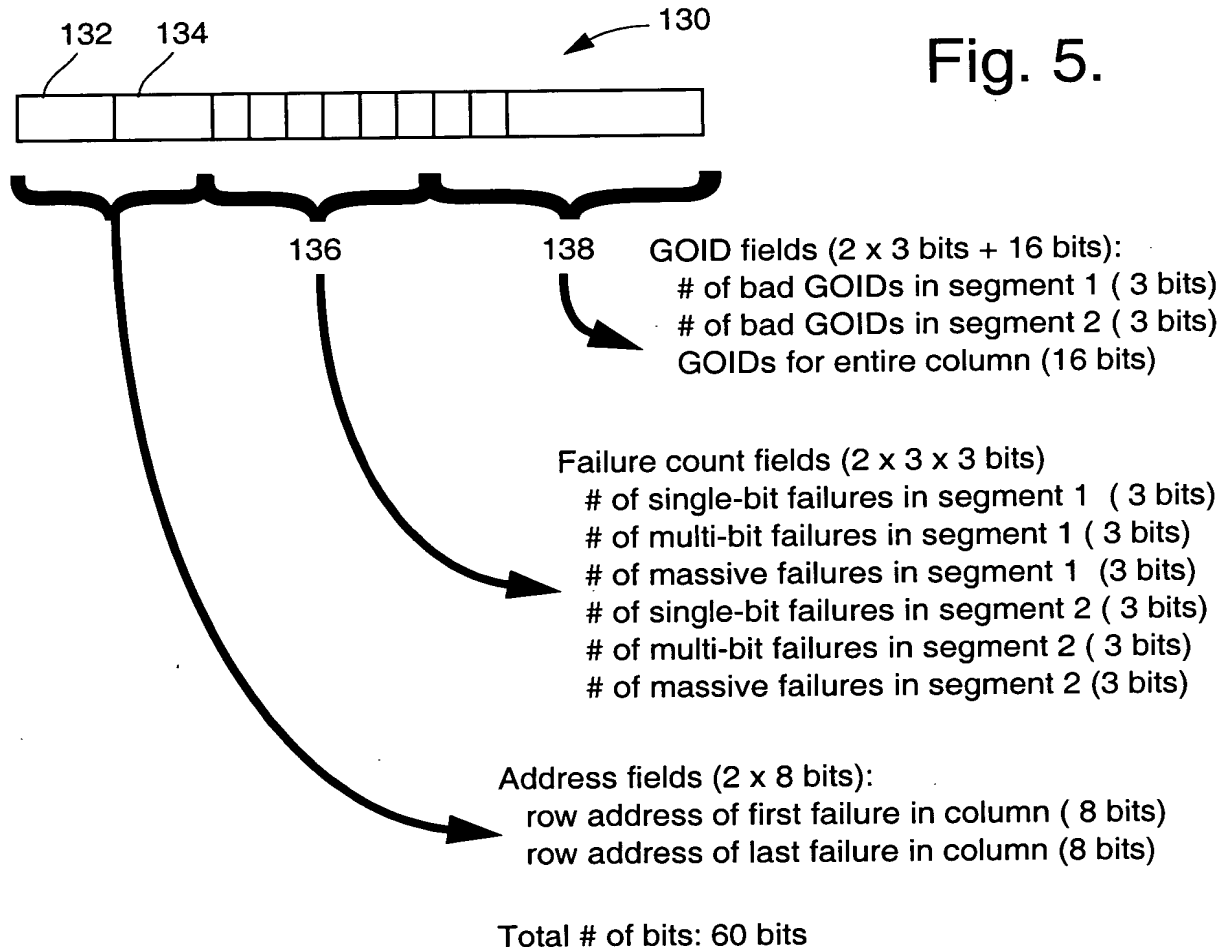
row addresses of first and last failure

failure counts: single-bit, multi-bit and massive failures

failure mask register information: number of bad bits

+Failure mask register contents for entire column: encoded for very wide memories. E.g. 64-bit word split into 8 groups of 8 bits. Only transfer register contents for 8 bits and identify group with a 3-bit field.

No row summary

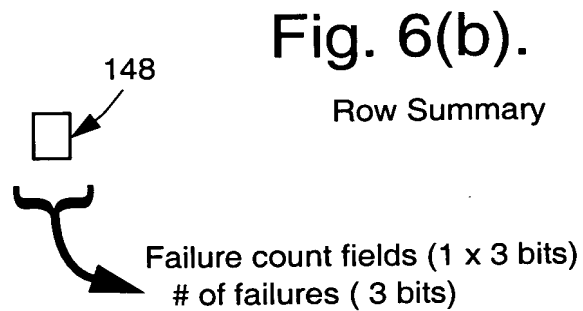
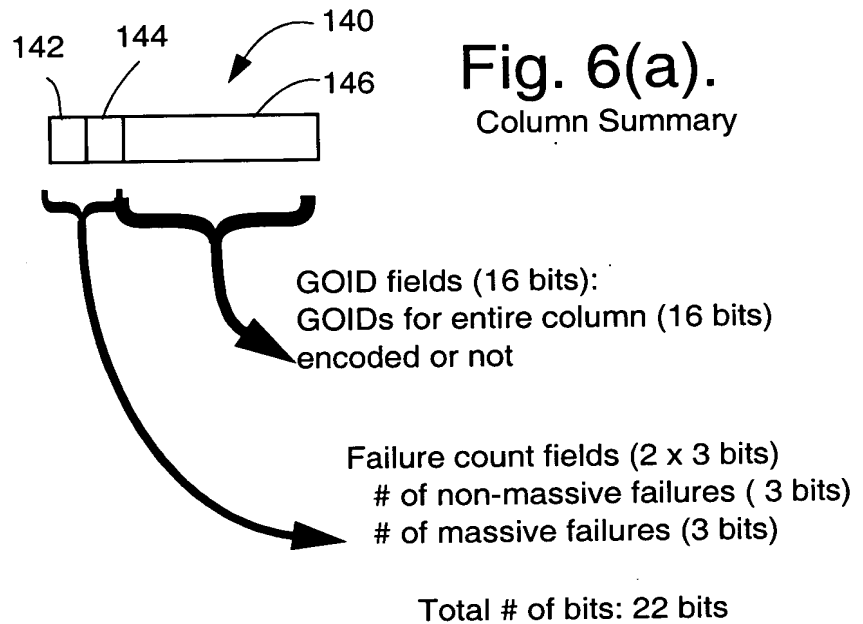


Column summary contains:

failure counts: massive and non-massive

failure mask register information: encoded or not

Row summary contains failure counts only



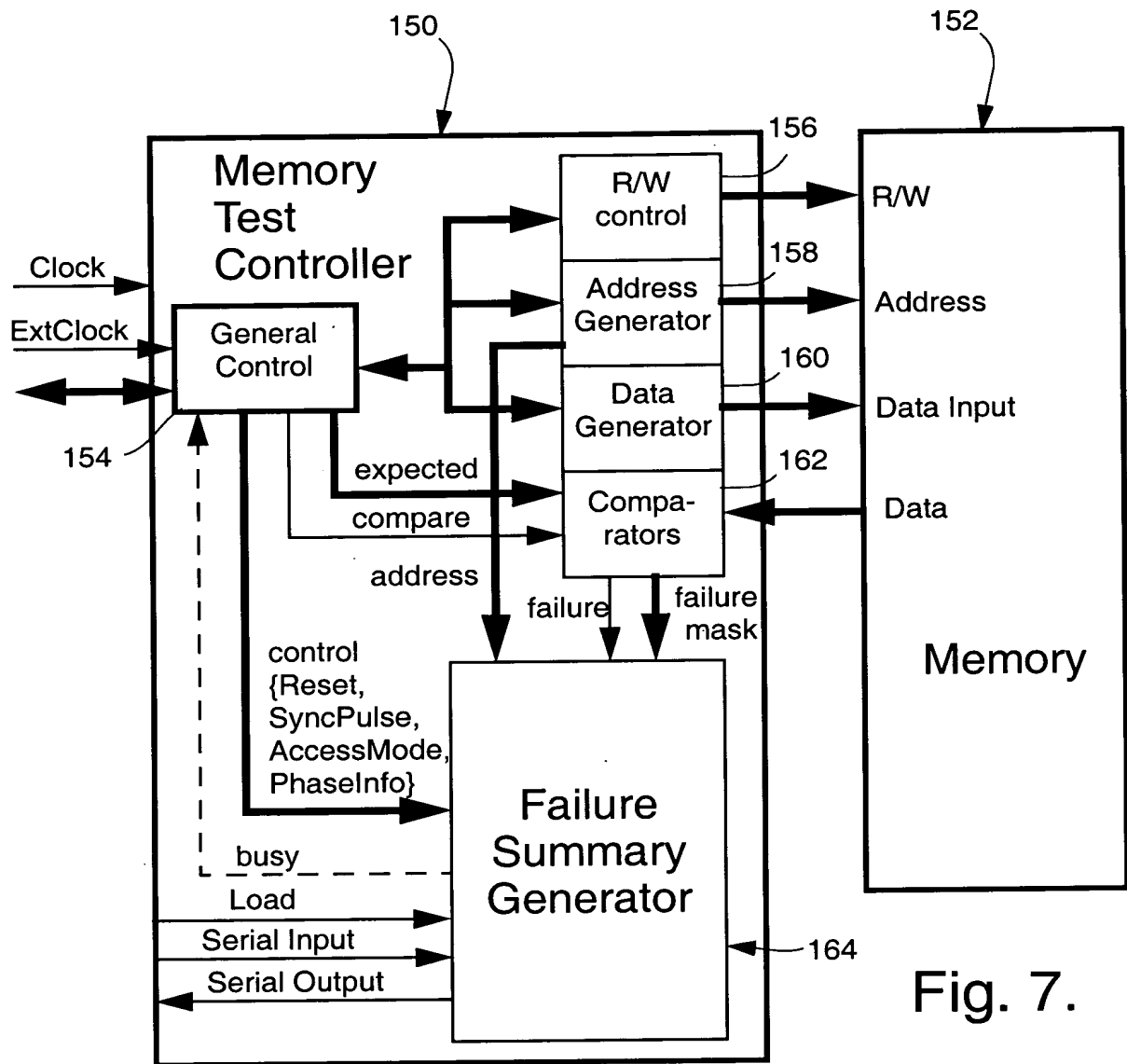
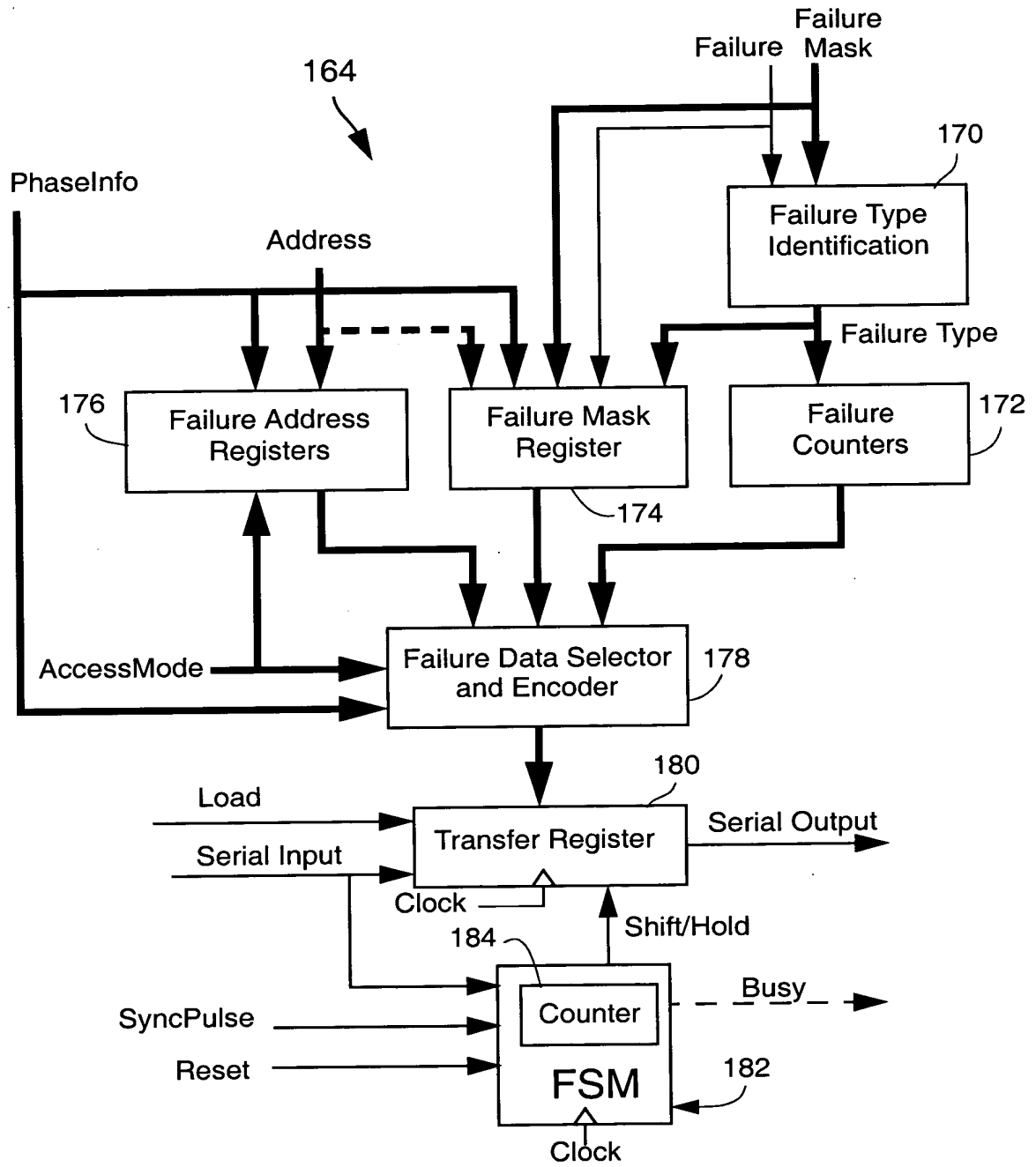


Fig. 8.



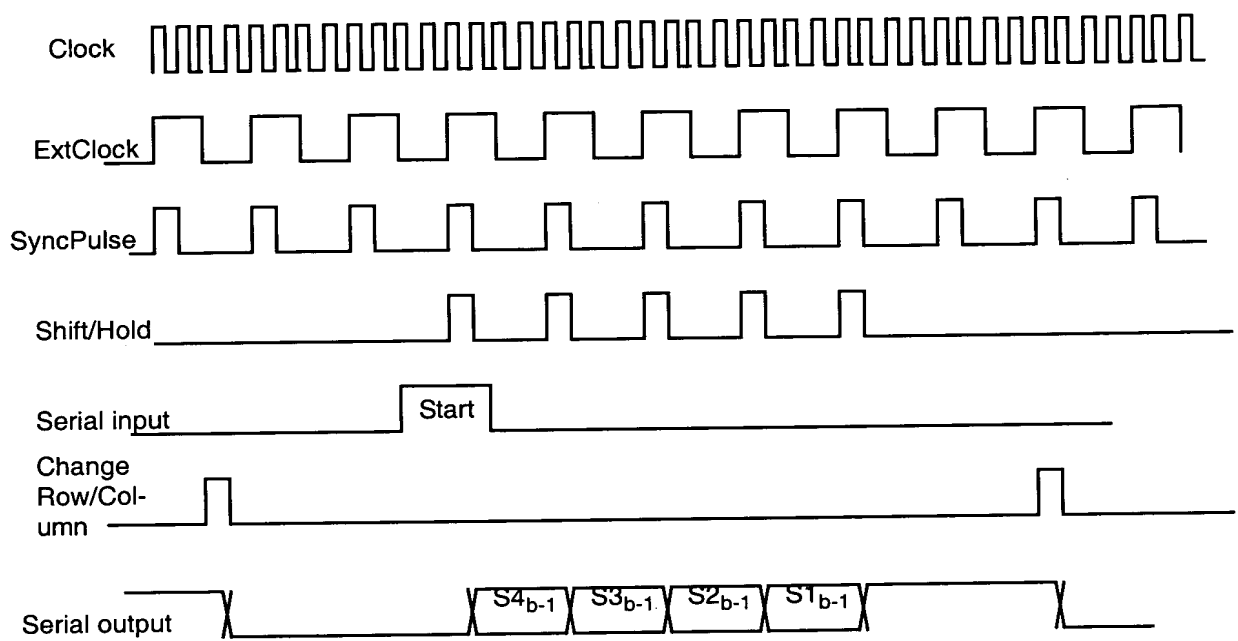


Fig. 9.

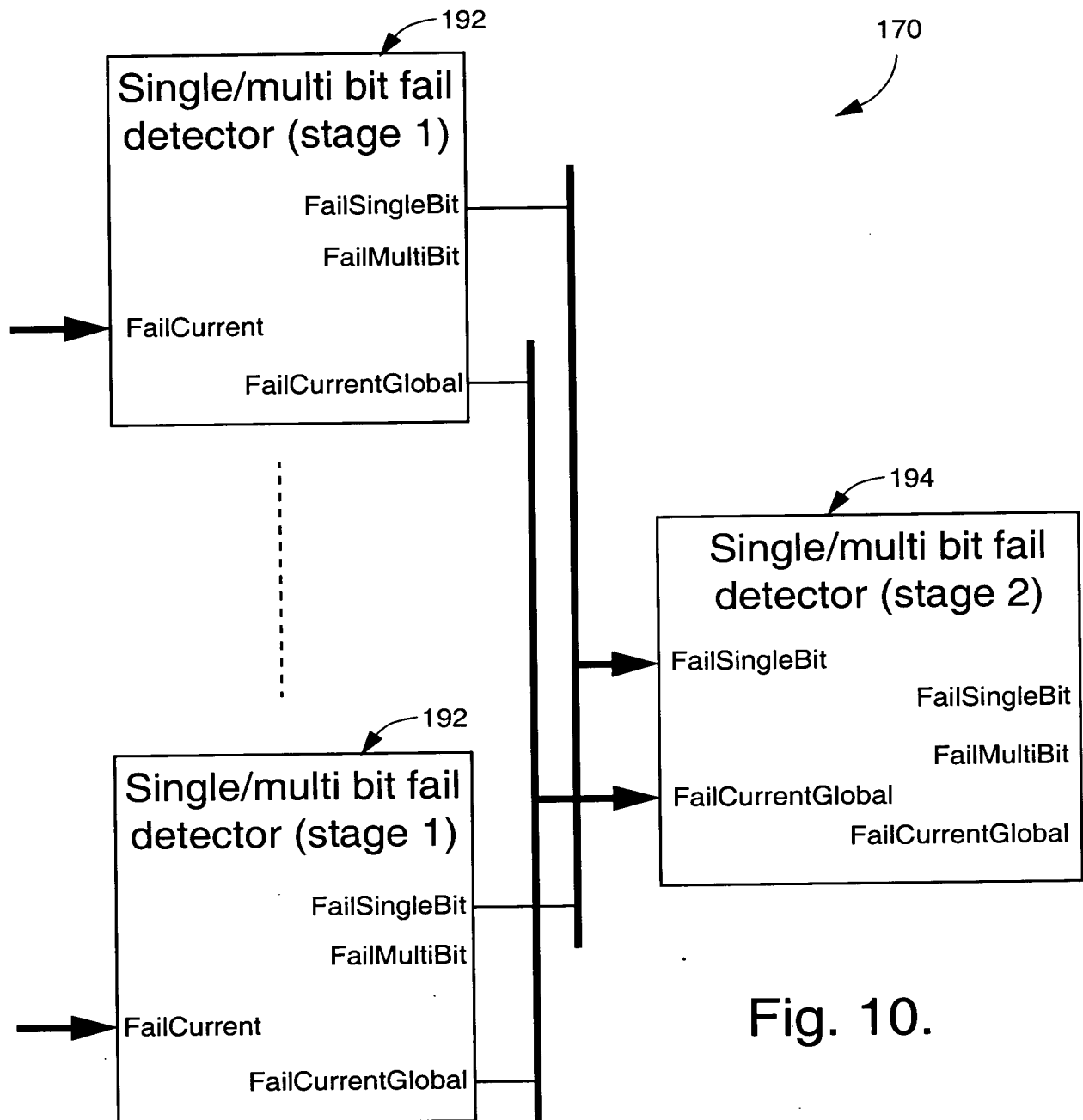


Fig. 10.

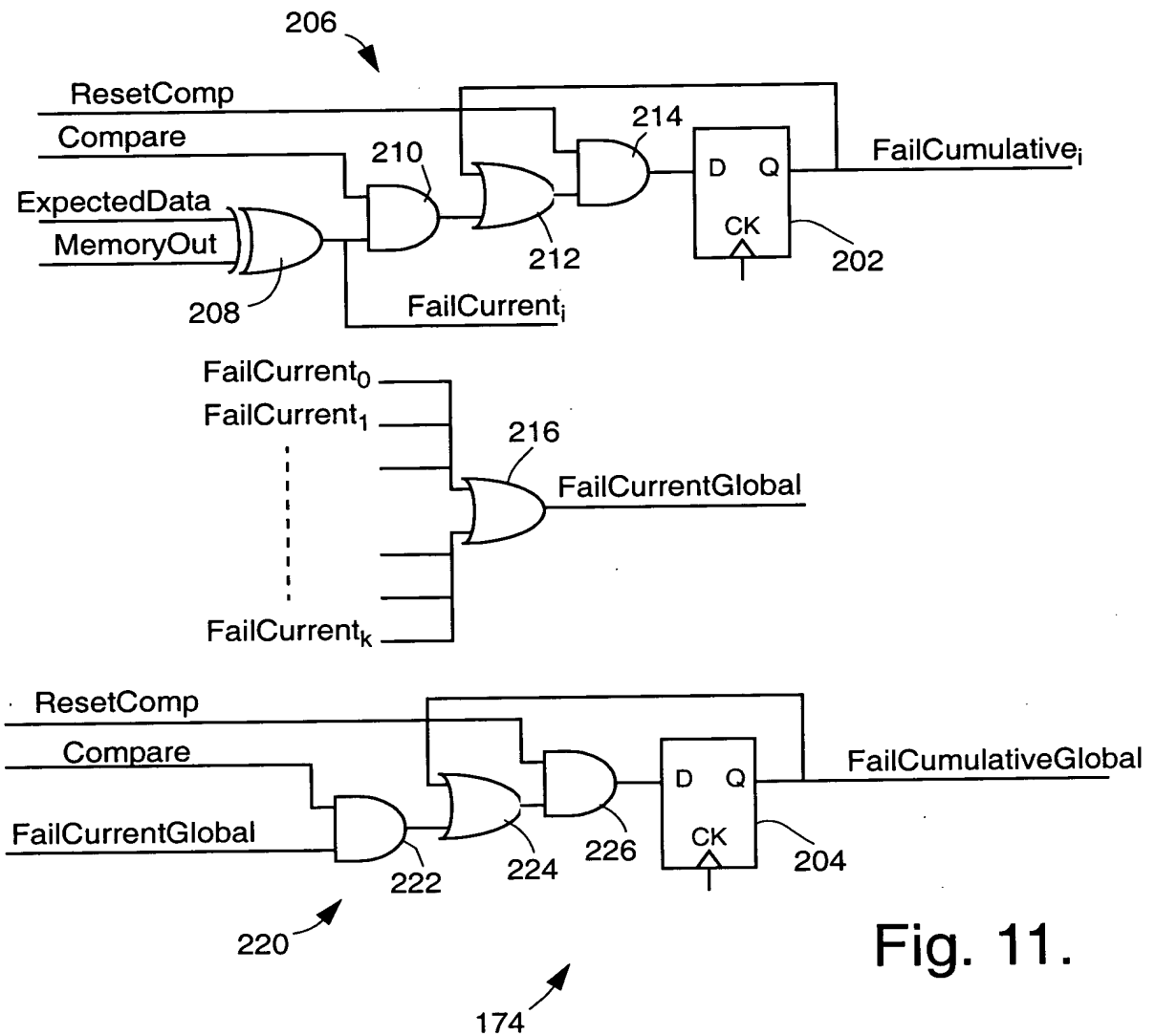
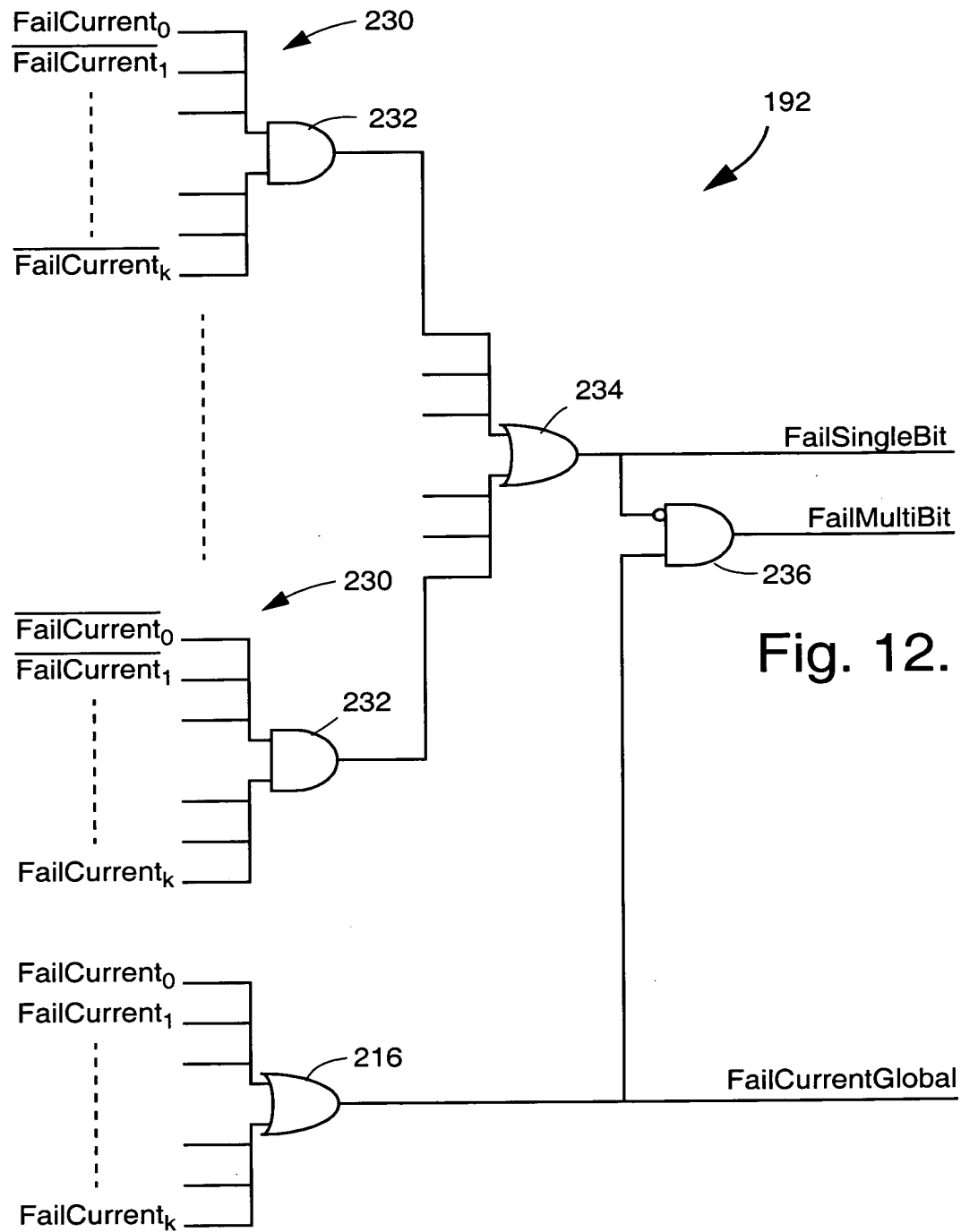
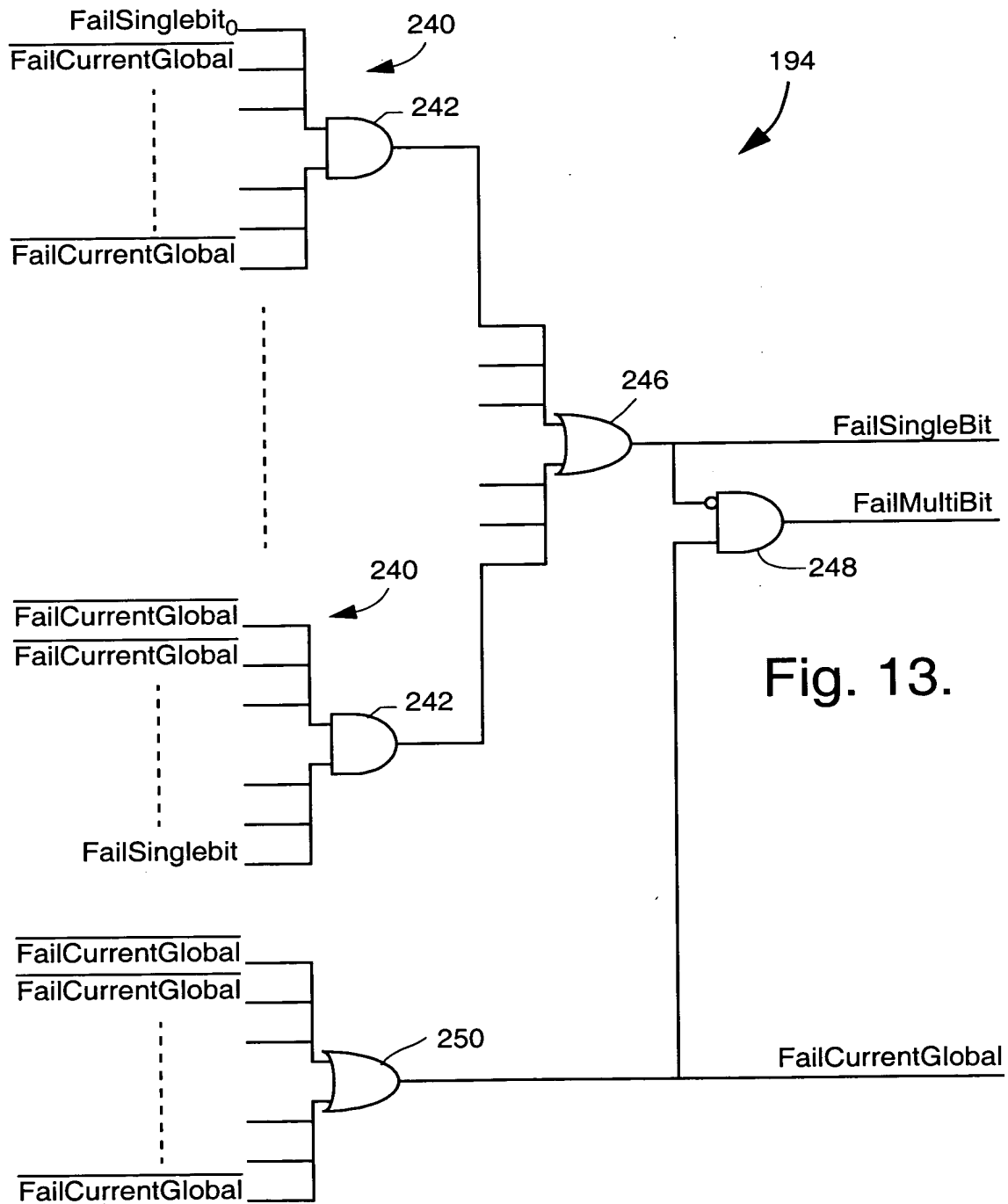


Fig. 11.





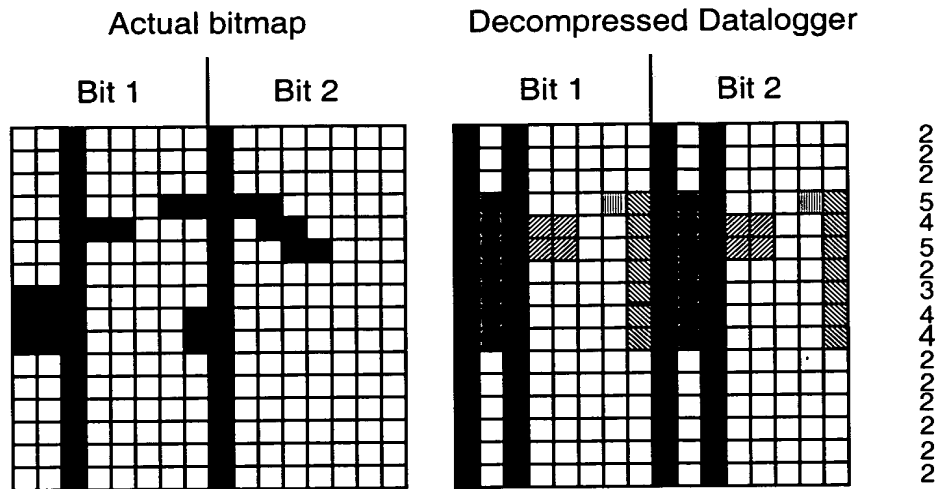
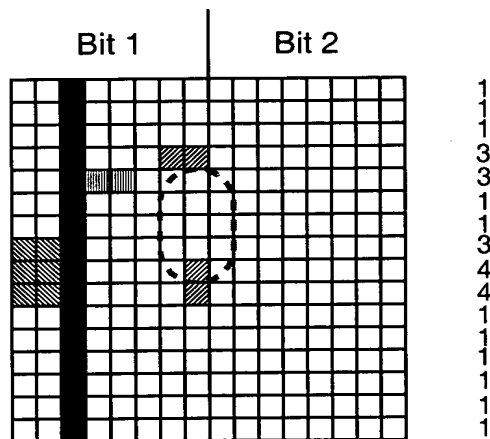


Fig. 14(a).

Area in dashed circled requires the row summary to resolve. All other portions only require column summary.



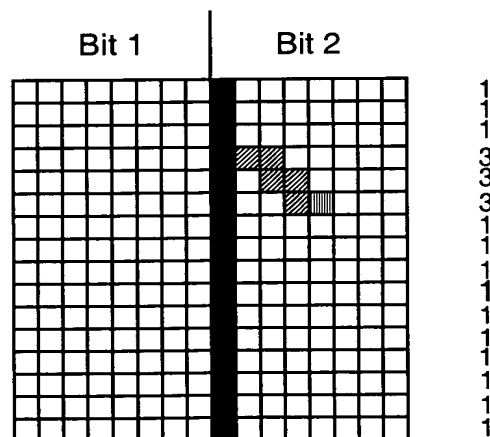
Pass 1

Fig. 14(b).

Pass 2, Bit 1

Fig. 14(c).

All failures for Bit 2 are resolved with the column summary



Pass 2, Bit 2

Fig. 14(d).

<input type="checkbox"/>	no fail	<input checked="" type="checkbox"/>	$3 < X < 25\%$ fail area	Code 4
<input checked="" type="checkbox"/>	1 fail area	<input checked="" type="checkbox"/>	$25\% < X < 50\%$ fail area	Code 5
<input checked="" type="checkbox"/>	2 fail area	<input type="checkbox"/>	$50\% < X < 100\%$ fail area	Code 6
<input checked="" type="checkbox"/>	3 fail area	<input checked="" type="checkbox"/>	100% fail area	Code 7

X - No. of Failures

Column Number	Pass 1	Pass 2 Bit 1	Pass 2 Bit 2
0	7 0 00 1 FF 1	3 0 07 1 09 1	7 0 00 1 FF 1
1	4 0 03 0 09 1	3 0 07 1 09 1	1 0 03 0 03 0
2	7 0 00 1 FF 1	7 0 00 1 FF 1	2 0 03 1 04 1
3	2 0 04 1 05 1	1 0 04 0 04 0	2 0 04 1 05 1
4	2 0 04 1 05 1	1 0 04 0 04 0	1 0 05 0 05 0
5	0 0 00 0 00 0	0 0 00 0 00 0	0 0 00 0 00 0
6	1 0 03 0 03 0	1 0 03 0 03 0	0 0 00 0 00 0
7	3 0 03 0 09 1	3 0 03 0 09 1	0 0 00 0 00 0

Fig. 14(e)

Pass 1	Pass 2 Bit 1	Pass 2 Bit 2
0110000000000000	0100000000000000	0010000000000000

Fig. 14(f)